EXTREMELY LOW POWER TRANSMITTER/RECEIVER GAAS MMIC CIRCUITS AT L BAND

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ABSTRACT

We have developed an Enhancement GaAs MMIC process which is capable of producing very low power, highly efficient transmitting/receiving circuits which can be operated from unipolar 3 V batteries. We have demonstrated key circuits such as a SAW locked oscillator, a Variable Gain 180° Phase Shifter and a Variable Gain Power Amplifier. The amplifier draws a dc current of 4 mA and delivers 4 dBm to 50 Ω loads with greater than 25 dB of gain.

INTRODUCTION

Many applications require low-power analog microwave circuits which consume low dc power and operate at low voltages. This is particularly true of handheld applications such as GPS, short range communication or inventory control systems in which the conservation of prime battery power is important. To address these applications, we developed a high performance, 0.5 μm gate length, ion-implanted enhancement GaAs process and demonstrated several key circuits. The process is capable of producing high gain devices with low knee voltages of less than 1 V which pinch-off at 0 V. The very low substrate losses and current leaks associated with the process allow us to design RF circuits in high impedance environments. Such environments are prerequisite to the efficient use of very small devices which consume low dc currents. Circuits made with such devices can easily be operated from unipolar 3 V batteries.

Ehancement MMIC Process

Circuits were fabricated using Raytheon's RF E/D process. The enhancement mode FET channel is formed by selective ion implantation of Si and Be. The unrecessed channel has a sheet resistance of 740 Ω/square, and a peak electron concentration of ~5 x 10^{17} cm^{-3}. The effective channel depth, prior to recessing, is ~1000 Å. The source and drain ohmic contacts are made on N^+ regions of the FET, which has a sheet resistance of 200 Ω/square. Gate material is Ti/Pt/Au and the recess depth is ~400 Å. Parasitic source and drain resistances are ~1.1 Ωmm.

The process also features GaAs implanted resistors with a sheet resistance of 740 Ω/square, low temperature coefficient (< 200 ppm/°C) 6 Ω/square TaN resistors, 300 pF/mm^2 MIM capacitors with 2000 Å SiN dielectric, air bridges, and low loss inductors and transmission lines with sheet resistance of 10 mΩ/square. The FETs have a nominal threshold voltage of 0.0 V with a standard deviation of 22 mV across a given 3 inch wafer. The maximum transconductance is 274 mS/mm at Vgs = 0.725 V. The gate breakdown voltage is > = 9 V.

Crystal-Locked Oscillator

The stability required of a transmitting system cannot be achieved with a free running oscillator at L band frequencies. We have designed and fabricated a Surface-Acoustic Wave (SAW) Locked oscillator which operates at UHF frequencies and selected its second harmonic for L band applications.

The schematics of the oscillator and a chip layout are shown in Figure 1a and 1b. The oscillator uses a modified iso-

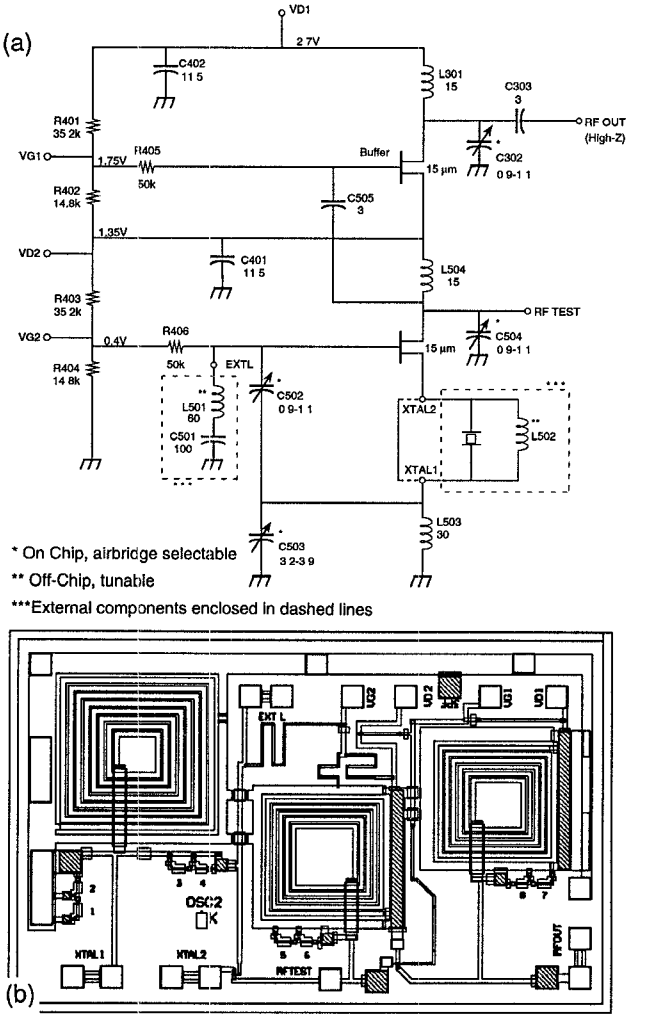

Figure 1. SAW Crystal Locked Oscillator/Multiplier; (a) Schematics, (b) Chip Layout. Shaded areas are capacitor tops.

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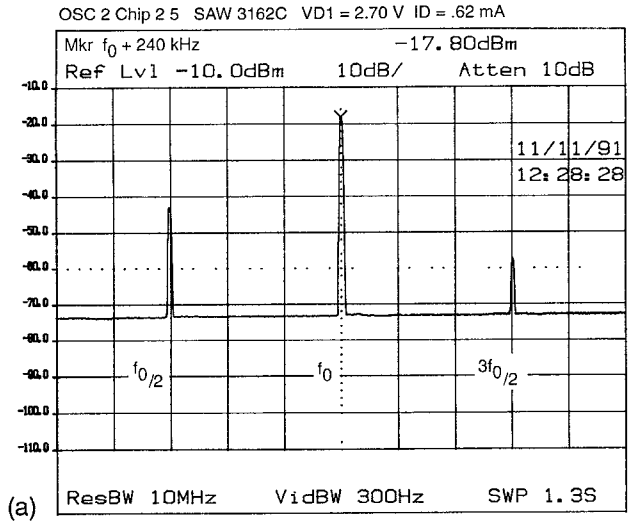
lated Colpitts topology and is designed to operate at UHF frequencies with a locking SAW crystal at the source of the oscillating FET. With the SAW shorted, the oscillator is designed to free-run at a frequency set by L501, C502 and L503/C503. A tuning range of ≈ 100 MHz (200 MHz at the 2nd harmonic at L band) is available by varying L501 which is an off chip air-core inductor. The exact frequency is set by the SAW crystal whose stray capacitance is neutralized by L502. The tank L504 C404 selects the second harmonic for amplification by the second FET which is connected in RF cascade and dc series to the oscillating FET. Both FETs are 15 μm in periphery. The totem pole connection reduces the dc current to a minimum. The resistors R401 to R404 insure that both FETs operate in their saturated regions.

Typical performance of the oscillator is shown in Figure 2 where both a wide and 10 KHz frequency spans are depicted in (a) and (b) respectively. The oscillator operates from a 2.7 V supply with a dc current of 0.6 mA and delivers -18 dBm of power. At 10 KHz away from its frequency, the noise is -105 dBm. The fundamental and 3rd harmonic suppressions are -23 and -40 dB respectively. The oscillator performs well, with reduced output, at supply voltages as low as 1 V.



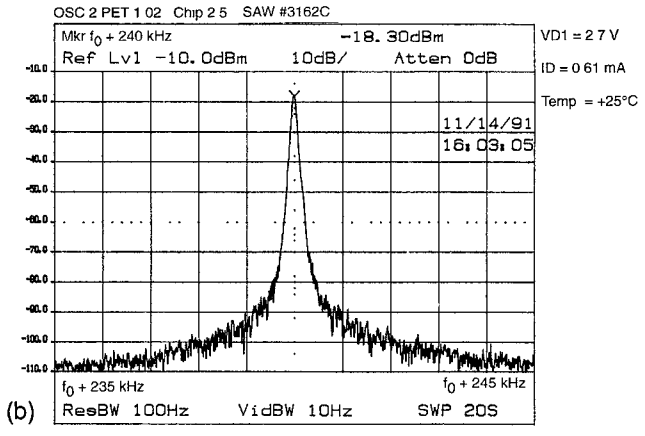


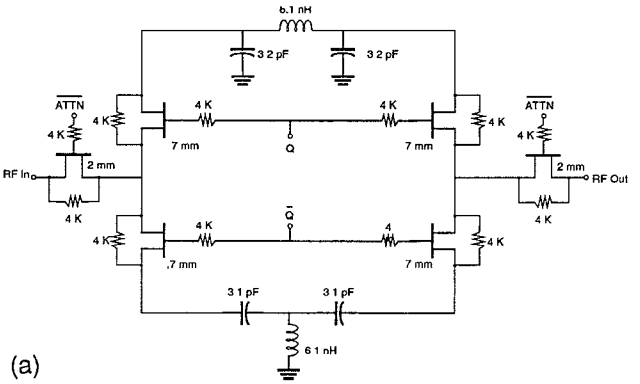
Figure 2. Performance of SAW Locked Oscillator/Multiplier; (a) Wide Band, (b) 10 KHz band.

Variable Attenuator/180° Phase Shifter

The 180° phase shifter uses a conventional high pass-low pass design to achieve the required phase shift. Switching between the low pass T and the high pass Π is performed by 700 μm wide switch FETs. The schematics of the circuit and a chip layout are shown in Figure 3a and 3b. The variable attenuation is achieved by 2 mm wide FETs connected in series with the input and output RF ports. 4 KΩ resistors are connected between the sources and drains of the FETs to insure operation in the linear regions of the devices. The phase control voltages Q and $\overline{Q}$ are 0 and 1 V and the analog attenuation control voltage varies between 0 and 0.7 V. Negligible current is required. Typical performance of the circuit is shown in Figure 4a through 4c. The phase shift is within 5° of 180° and within 1 dB of amplitude balance over the 950 MHz to 1250 MHz frequency range. The attenuation range varies between 35 dB at 800 MHz and 25 dB at 1300 MHz. The minimum insertion loss is 4 dB.

Variable Gain Power Amplifier

A Variable Gain Three Stage Amplifier shown schematically in Figure 5a has been designed and built. A chip layout is



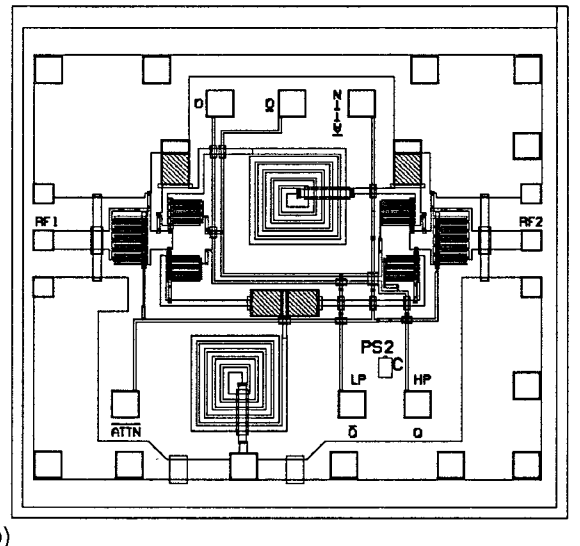


Figure 3. Variable Attenuation/180° Phase Shifter; (a) Schematics, (b) Chip Layout. Shaded areas are capacitor tops.

shown in Figure 5b. The FETs in the three stages are 20, 30 and 80 μm wide, respectively. The first two stages use FETs of the same sizes as active RF loads. The use of active loads achieves high gain and low dc power consumption since it provides high RF to dc isolation with lower loss of voltage when compared to the use of resistors. The use of active loads requires that both devices remain in their saturated regions under all conditions of processing variations and gain control biasing. Such stable biasing arrangement is provided by resistors R19 to R22 and R23 to R26 in the two stages, respectively. To keep the current consumption of the amplifier to a minimum, we opted to use off chip air-core RF chokes for biasing the drain of the output power FET.

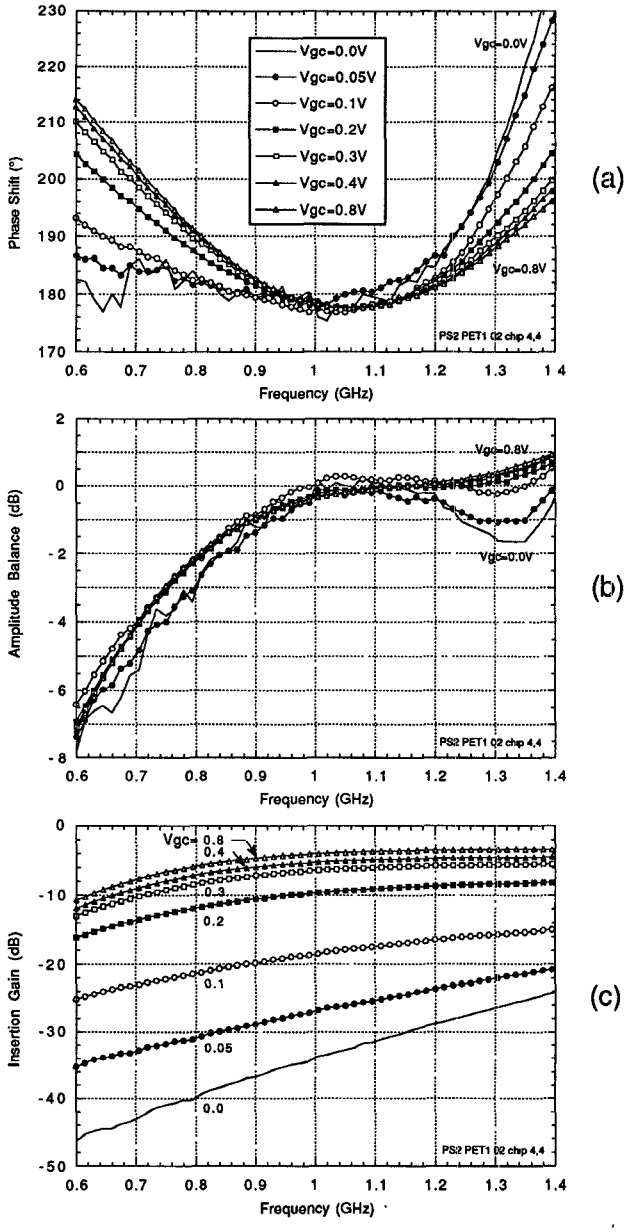


Figure 4. Frequency Performance of Variable Attenuation 180° Phase Shifter Parameterized by Attenuation Control Voltage Vgc; (a) Phase Shift, (b) Amplitude Balance, (c) Attenuation.

The frequency performance of a typical amplifier at an input power of -25 dBm with the gain control voltages varying between 0.6 and -0.1 V is shown in Figure 6. The amplifier shows a maximum gain of 28 dB with a 30% bandwidth at low L band. A gain control range of 18 dB is indicated when Vgc varies between 0 and 0.6 V, an extra 5 dB of gain control is available when Vgc = - 0.1 V. The power performance of the amplifier at a fixed frequency with a dc supply of 2.7 V is shown in Figure 7a through 7d. All the figures are parameterized by the gain control voltage Vgc which varies between 0 and 0.6 V. Maximum power of 4.5 dB is delivered to the 50 Ω load at a gain of 29 dB with Vgc = 0.6 V. In this case, the dc current is 4.5 mA and the power added efficiency is 20%. Maximum efficiency of 25% can be obtained with Vgc = 0.4 V. The delivered power is 4.5 dBm, the dc current is 3.8 mA

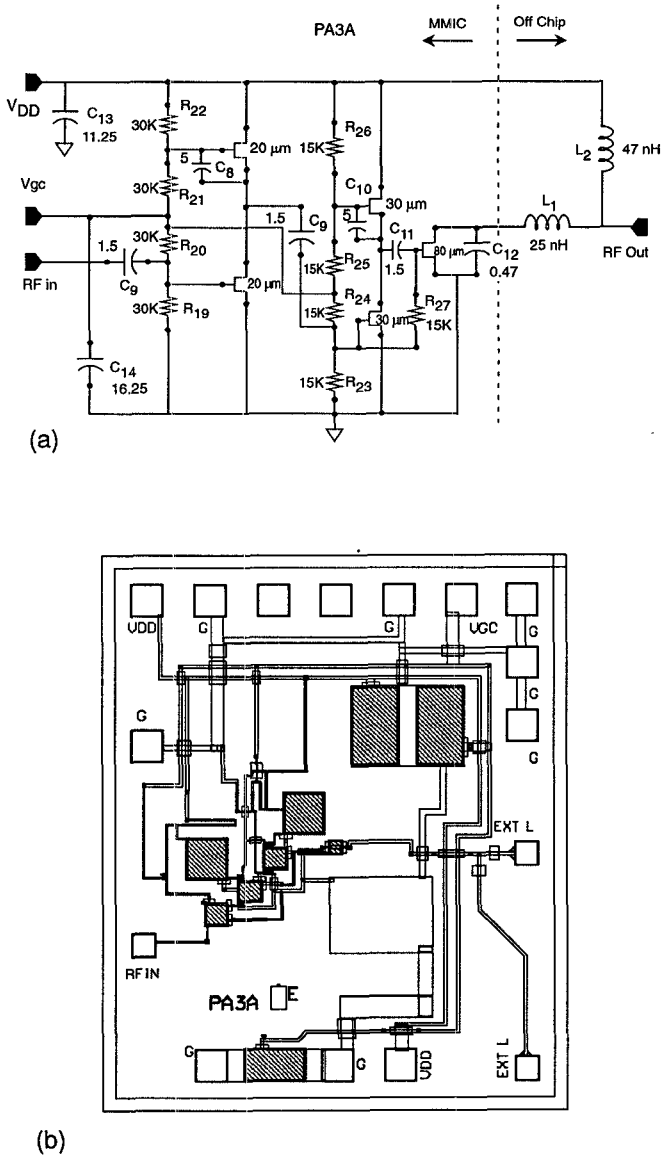


Figure 5. Variable Gain Three Stage Power Amplifier; (a) Schematics, (b) Chip Layout.

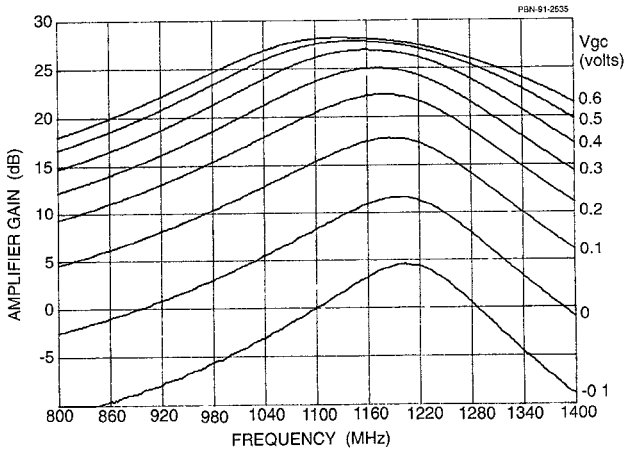


Figure 6. Frequency Response of Variable Gain Three Stage Amplifier at an Input Power of -25 dBm Parameterized by Gain Control Voltage Vgc.

and the gain is 24 dB. Notice that the dc current consumption decreases with decreased gain. At Vgc = 0 V a minimum of 1 mA of current is achieved. In this case, -14 dBm is delivered to the load with a gain of 11 dB.

CONCLUSION

We have developed a process which is capable of producing very low power highly efficient transmitting and receiving circuits in MMIC form which can be operated from unipolar single batteries. We have demonstrated several such circuits which can be used in many hand-held commercial applications where the preservation of battery life is important.

Acknowledgements

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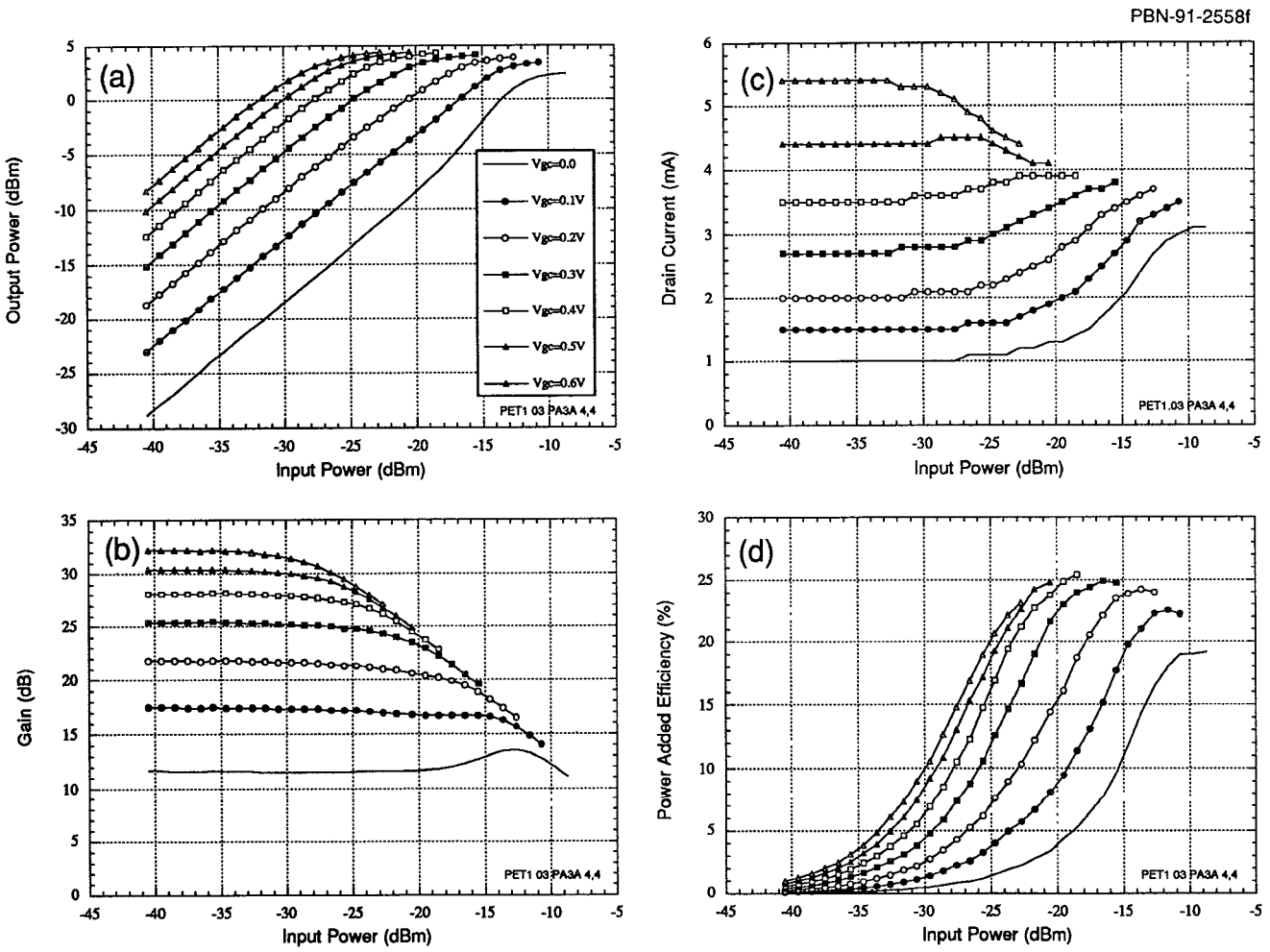

Figure 7. Performance of Variable Gain Power Amplifier as a Function of Input Power at Fixed Frequency Parameterized by Control Voltage Vgc with Vds = 2.7 V; (a) Output Power, (b) Gain, (c) Drain Current, (d) Power Added Efficiency.